REMARKS

Claims 31, 32, and 38-54 remain pending in this application. Applicants acknowledge that the Examiner has withdrawn all previous objections and rejections to the claims.

In the Final Office Action dated October 5, 2005, the Examiner rejected claims 31, 32 and 38-54 under 35 U.S.C. 112, second paragraph, asserting indefiniteness. Applicants respectfully traverse this rejection. Applicants respectfully assert that the term "at least two of said plurality of data lines are latched from respective memory portions" is readily understood by those skilled in the art as having respective relationship with respective memory portions. The "plurality of data lines" are part of the memory device and contrary to the Examiner's assertion, there's not need to specifically recite that different portion of the memory have their own data lines to be definite. It would be clear to those skilled in the art that at least two of the plurality of data lines are latched from two respective memory portions, without having to recite that each memory portion has its own data lines. Further, there is no evidence or persuasive arguments to support Examiner's contention that the term "respective" requires a prior indication of memory elements being related to some other element. *See*, page 2 of the Final Office Action dated October 5, 2005. In the context of the claim language is would be clear and definite to those skilled in the art that two of the data lines are latched from two respective memory portion. In the ordinary use of this term, it would be clear to those skilled in the art that this term refers to one of the data lines being latched from one memory portion and the other data line being latched from another memory portion, which is clearly provided by the phrase "wherein at least two of said plurality of data lines are latched from two respective memory portions" in claims 31 and

38. Accordingly all of the term of claims 31 and 38 are definite and meet the entire requirement of 35 U.S.C. 112, second paragraph. Hence, claims 31 and 38 are allowable.

The Examiner rejected claims 31, 32 and 38-54 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,311,299 ***(Bunker)***. In light of the arguments provided herein, Applicants respectfully traverse this rejection.

Applicants respectfully assert that in the Final Office Action dated October 5, 2005, the Examiner erred in interpreting the disclosure in ***Bunker***. In particular, for example, the Examiner asserted that the compression circuits DC1 through DC8 do not correspond separately to the various memory arrays A1 through A8. *See*, paragraph 4, on page 5, of the Final Office Action dated October 5, 2005. Applicants respectfully assert that the Examiner misinterpreted the disclosure of Figure 2. Although Figure 2 is a stylized illustration that provides a test circuitry 206, which includes the compression circuits DC1-DC8, 246a-246h, for convenience, the Figure itself merely illustrates DC8 and DC1. Perhaps this has caused some confusion as to whether a compression circuit is respectfully corresponding to a memory array. However, the description in ***Bunker*** clarifies this issue. For example, the description in ***Bunker*** states that each of the data compression circuits DC1-DC8 receives a respective bit of lead data applied on the data path from each of the arrays A1-A8. *See* column 5, lines 23-24. Thus, it is clear that a data compression circuit in ***Bunker*** relates to an array in a respective manner. Therefore, it is abundantly clear that ***Bunker*** provides for a compression circuit to separately compress one of the memory arrays. This is in contrast with claim 31, which recites a method, which calls for a compressing circuit to compress data from at least two memory portions (as described in further detail below). The Examiner has misinterpreted the use of the compression circuits and the

memory arrays of Figure 2 to misapply the subject matter of ***Bunker*** to argue anticipation of the elements of claim 31 of the present invention. These arguments are described in further detail below.

The Examiner also states that "...the bottom line is the compression circuit comprising sub circuits DC1-DC8 in Figure 2, is still a compression circuit." This is a misapplication of the disclosure of ***Bunker***. Actually, what ***Bunker*** discloses is that the test circuitry 206 includes a plurality of data compression circuits DC1-DC8, 246A-246H. *See* column 5, lines 23-24. This is yet another example of the Examiner's misapplication of the disclosure of ***Bunker***. As described below, ***Bunker*** clearly does not anticipate a compressing circuit to compress data from at least two memory portions. Various advantages disclosed by the present application is also cited below, wherein these advantages are not available in the system disclosed in ***Bunker***. (See detailed descriptions of these arguments below).

Additionally, in the Final Office Action dated October 5, 2005, the Examiner asserted that the Applicants' contention is "absurd". *See* second paragraph of page 6, of Final Office Action dated October 5, 2005. Applicants are saddened by this comment and respectfully disagree with the Examiner's characterization of Applicants' arguments. The Examiner asserts that there are various cross-connections. For example, the Examiner cites that memory array A1 may correspond to compression circuit DC3 just as much as A5 corresponds to DC3 due to the connections of the IO lines. However, the eight compression circuits described in ***Bunker*** respectfully correspond to one of the eight arrays disclosed by ***Bunker*** in Figure 2. Applicants did not argue that a compression circuit (*e.g.*, DC5) must necessarily correspond to a similarly numbered memory array (*e.g.*, memory array number 5), even though it may be a possibility.

However, Applicants have proven by citing disclosure in ***Bunker*** that the compression circuits, DC1-DC8, receive respective bit of read data applied to data compression circuit from each of the arrays as called for by claim 1 of the present invention A1-A8. *See* column 5, lines 29-31. Simply because a data box may be shared does not mean that a memory array strictly only corresponds to a particular compression circuit. If the Examiner's logic were followed, then there would be no real need for eight compression circuits that somehow correspond to eight memory arrays. However, contrary to the Examiner's assertions, ***Bunker*** actually discloses eight compression circuits that correspond to eight memory arrays.

Additionally, the Examiner's attempt at grouping these into one large compression circuit is flawed since ***Bunker*** specifically cites in Figure 2, as well as in the Specification of ***Bunker***, that the test circuitry 206 includes a plurality of compression circuits DC1-DC8. *See* column 5, lines 23-24. Applicants respectfully assert that the Examiner's arguments are in error and that ***Bunker*** clearly does not disclose the compression circuit elements called for by claim 31 of the present invention. These arguments are further detailed below.

Regarding the element of latching data present on at least a subset of the plurality of data lines called for by claim 31 of the present invention, the Examiner has, again, misconstrued the disclosure of ***Bunker***. For example, the Examiner argued that the flip-flops HFF1-HFF8 and the buffers BUF1-BUF8 associated with each of the data masking circuits of ***Bunker*** are a plurality of data latches for use to matching data on a subset plurality of data lines. *See*, first paragraph of page 7 of the Final Office Action dated October 5, 2005. The Examiner had failed to consider that the element of claim 31 further recites that at least two of the plurality of data lines are latched from two respective memory portions, the HFF and the buffers cited by the Examiner

merely latches different data lines from the same memory portion, *i.e.*, from either array 1 or one of array 2 through array 8. In other words, ***Bunker*** does not disclose the latching of the data present on at least a subset of a plurality of data lines wherein at least two of the plurality of data lines are latched from two memory portions. ***Bunker*** merely latches data from any one of the memory portions or arrays A1-A8. Therefore, this is another claim element that is not taught, disclosed or suggested by ***Bunker***. These arguments are further detailed below.

In the Final Office Action dated October 5, 2005, regarding the element of compressing data to determine that the data matches a predetermined pattern as being anticipated, Applicants respectfully assert that the Examiner has again erred in interpreting the disclosure of ***Bunker***. For example, the Examiner cites the abstract, which recites that each data compression circuit compares each of the data signal applied to a respective input to an expected value and generates an active error signal. The Examiner uses this disclosure to read upon the matching of the predetermined pattern called for be claim 31. However, this passage in ***Bunker*** is further detailed and clarified as to how the error signals E1-E8 are generated. ***Bunker*** clearly describes that each of the data compression circuits, DC1-DC8, determines whether each of the bits applied on its inputs has the same binary value, and generates a corresponding error signal E1-E8 in response to this determination. *See* column 5 lines 32-35. Further, ***Bunker*** discloses that when each of the applied read data bits has the same binary value, each of the data compression circuits, DC1-DC8, drives its corresponding error signal E1-E8 inactive...". *See* column 5, lines 38-41. Therefore, the Examiner is in error as to how the error signals E1-E8 are generated. Rather than determining whether the mass data matches a predetermined pattern, ***Bunker*** is

directed to determining whether each of the bits applied to the inputs of the compression circuits has the same binary value.

The data compression circuits, which includes circuitry to compare each of the applied read bits to a corresponding predetermined value disclosure in ***Bunker***, is not sufficient enabling disclosure to anticipate all of the elements of claims 31 and 38 of the present invention. As described in further details below, simply disclosing that the data compression circuits may include circuitry to compare each of the applied read bits does not disclose or anticipate compressing the data to determine if the data matches a predetermined pattern. As described herein, ***Bunker*** does not disclose latching data present on a subset of a plurality of lines in latch form to respective memory portions and masking the data and compressing the mass data to determine whether it matches a predetermined pattern, as called for by claims 31 and 38 of the present invention. ***Bunker*** merely masks data using separate data masking circuitry DM1-DM8 that correspond to array A1-A8. Therefore, ***Bunker*** does not mask data lines from at least a subset of a plurality of data lines from two respective memory portions. Therefore, ***Bunker*** couldn't possibly disclose compressing that mass data and comparing it to a predetermined pattern. These arguments are further detailed below.

As described above, claim 31 calls for latching a plurality of data lines, wherein two data lines are latched from two respective memory portions. Claim 31 also calls for masking the latched data lines and compressing the masked data lines using a compression circuit. Therefore, claim 31 calls for compressing latched data lines where at least two of the data lines from two different memory portions are compressed by a compressing unit. In contrast to claim 31, ***Bunker*** discloses a system where each memory array (A1-A8) corresponds with a particular data

compression circuit (DC1-DC8). In other words, ***Bunker*** discloses that data from each memory array must be compressed by a separate, corresponding compression circuit. *See*, Figure 2, column 5, lines 23-35. In contrast to ***Bunker***, claim 31 recites a method that calls for a compressing circuit to compress data from at least two memory portions. Various advantages provided by the method in claim 31 is described in the specification, which includes but is not limited to, allowing a compression to be shared by a plurality of memory portion, *e.g.*, memory core, allowing for ease of re-design of memory, e.g., increasing memory density without adding additional compressing circuit. *See* for example, page 12, lines 5-15 of the Specification. These advantages would not be available in the system disclosed in ***Bunker***.

The system in ***Bunker*** clearly describes that each memory portion requires a corresponding compression circuit. This disclosure does not anticipate or make obvious the method recited in claim 31, which calls for a compressing circuit to compress data from at least two memory portions. Therefore, for at least this reason, all of the elements of claim 31 are not anticipated or made obvious by ***Bunker***. Additionally, independent claim 38 calls for means for masking the latched data lines and means for compressing the masked data lines using a compression circuit. For at least the reasons cited above, claim 38 is also not anticipated by ***Bunker*** since ***Bunker*** requires that each memory portion be associated with a corresponding compressing/compression circuit. Therefore, claim 38 is also allowable for at least the reasons cited above.

There are additional reasons that support Applicants' assertions that claims 31 and 38 of the present invention are allowable over ***Bunker***. For example, ***Bunker*** discloses a plurality of data masking circuits, DM1, DM2, that are coupled to particular arrays, A1 and A2. *See*, Figure

2, column 4, lines 14-19. The masking function disclosed by ***Bunker*** merely receives an array of data for each masking circuit, wherein one or more of the data lines called for by claim 31 of the present invention, is masked based upon an enable signal. Therefore, the disclosure of ***Bunker*** does not read upon all of the elements of claim 31.

Further, the function performed by the compression circuits DC1-DC8 disclosed by ***Bunker*** all receive a respective bit of read data that is applied on the data above from each of the arrays A1-A8. *See,* column 5, lines 29-31. The compression circuits DC1-DC8 make a determination whether each of the bits applied upon its inputs has the same binary value and generates an error signal E1-E8 in response. *See,* column 5, lines 31-35. ***Bunker*** discloses that if any of the applied read data bits applied to the compensation compression circuit DC1-DC8, has a binary value different from that of the other applied data bits, the error signal is generated. In contrast to ***Bunker***, the compression circuit called for by claim 31 of the present invention calls for detecting a predetermined pattern on a subset of data lines and to provide a pass signal when the predetermined pattern is detected on the subset of data lines. Therefore, ***Bunker*** does not disclose performing the detection of the predetermined pattern, as called for by claim 1 of the present invention.

Bunker merely discloses comparing the binary value of the bits of the compensation circuit DC1-DC8 to determine whether they are equal in value, therefore, the predetermined pattern detection is not performed or disclosed by ***Bunker***. Hence, another aspect of the elements of claim 1 are not disclosed, taught, or suggested by ***Bunker***. ***Bunker*** discloses that in the masking mode, which is the mode used to read upon the claims of the present invention, when the data bit from the masking circuit is masked, the compression circuit compares the

binary value of the bits from all other masking circuits and generates an error signal in response to this comparison. This is performed for individual masking circuitry and compression circuits. *See,* column 7, lines 2-6. It is clear that the system of ***Bunker*** discloses comparing binary values from other masking circuits by the compression circuit to generate an error signal. In contrast, claim 31 calls for detecting a predetermined pattern on a subset of data lines to determine whether a pass signal is to be provided based upon comparison to a predetermined pattern. This is not taught, disclosed, or suggested by ***Bunker***, which relies on comparing binary values of each bit applied to the inputs of the compression circuits DC1-DC8 to determine that an error signal is asserted. Therefore, ***Bunker*** does not disclose, teach, or suggest, all of the elements of claim 1 of the present invention.

In contrast to ***Bunker***, claim 31 calls for compressing the masked data to determine if the masked data actually matches a predetermined pattern. ***Bunker*** discloses that the test circuitry operates during a first test mode to compress test data from a plurality of memory cell arrays to generate an error signal. ***Bunker*** does not disclose compressing mask data if the mask data matches a predetermined pattern. ***Bunker*** discloses that data compression circuits include circuitry to compare each of the read data bits to see if it has a binary value different from that of other applied read data bits. However, ***Bunker*** does not disclose compressing the masked data to determine if the mask data matches a predetermined pattern.

The Examiner cites column 5, lines 54-57 in ***Bunker*** to assert that it teaches that the masked data is compressed within the compression circuit DC1-DC8 by comparing each of the applied read mask bits to a predetermined value to determine if the applied read matches the predetermined value. However, Applicants respectfully assert that column 5, lines 54-57,

discloses that the data compression circuits may include circuitry to compare each of the applied read data bits to a corresponding predetermined value, which may then be used to generate an error signal. However, ***Bunker*** does not disclose compressing the mask data to determine if the mask data matches the predetermined pattern. ***Bunker*** provides data into different arrays A1-A8 into the masking circuit. In contrast, claim 31 calls for latching data present on a subset of plurality of data lines and masking the data, wherein each masking circuit is provided an array of data according to ***Bunker***, which is not taught or suggested by ***Bunker***. Furthermore, claim 31 calls for compressing the masked data to determine if the masked data matches the predetermined pattern to provide a pass signal if there is a match. ***Bunker*** does not disclose compressing the masked data to determine if the masked data matches a predetermined pattern. ***Bunker*** merely discloses that the data compression circuit examines whether the binary value of a read bit is different from that of another read bit. Accordingly, all of the elements of claim 31 are not disclosed, taught, or suggested by ***Bunker***. Additionally, claim 38 provides for a means plus function apparatus claim that calls for means for performing the similar function(s) described previously. Therefore, it is not taught, disclosed, or suggested by ***Bunker***. Therefore, claim 38 is also allowable for at least the reasons cited above.

Independent claims 31 and 38, are allowable for at least the reasons cited above. Additionally, dependent claims 32, and 39-54, which depend from independent claims 31 and 38, respectively, are also allowable for at least the reasons cited above.

The Examiner rejected claims 31, 32 and 38-54 under 35 U.S.C. 102(f) asserting that the Applicants did not invent the claimed subject matter in view of U.S. Patent No. 6,311,299 (***Bunker***)". Applicants respectfully traverse this rejection.

As described above, independent claims 31 and 38 refer to compressing latched data lines where at least two of the data lines from two different memory portions are compressed by a compressing unit. These elements are not taught, disclosed, or suggested by ***Bunker***. Therefore, ***Bunker*** could not be prior art to claims of the present invention. Hence, Applicants respectfully assert that Examiner's assertion that Applicants did not invent the claimed subject matter is incorrect.

Additionally, as described above, ***Bunker*** does not disclose all of the elements of claims 31 and 38; for example, ***Bunker*** does not disclose compressing the masked data to determine if the masked data matches a predetermined pattern. Claim 31 calls for compressing the masked data to determine if the masked data matches a predetermined pattern, wherein ***Bunker*** is directed to a test circuitry that operates during a first test mode to compress test data from a plurality of memory cell arrays to generate an error signal. Further, ***Bunker*** discloses compressing an unmasked bit, wherein claims 31 and 38 call for compressing a masked bit, which is yet another example of the reasons why ***Bunker*** does not anticipate claims 31 and 38 of the present invention. Other examples of the reasons why ***Bunker*** does not disclose all of the elements of claims 31 and 38 are provided above in the previous section. Therefore, claims 31 and 38 are allowable for at least the reasons cited above.

Independent claims 31 and 38, are allowable for at least the reasons cited above. Additionally, dependent claims 32 and 38-54, which depend from independent claim 31, are also allowable for at least the reasons cited above.

Reconsideration of the present application is respectfully requested.

In light of the arguments presented above, Applicants respectfully assert that claims 31, 32, and 38-54 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the **Examiner is requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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